Vertical cavity surface emitting lasers utilizing native oxide mirrors and buried tunnel contact junctions

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Vertical cavity surface emitting lasers (VCSELs) are demonstrated with high-index-contrast native-oxide-based (Al\textsubscript{x}O\textsubscript{y}) distributed Bragg reflectors (DBRs) on both sides of a ‘‘2X’’ cavity, thus creating a compact (thick, ~2.8 \( \mu \)m) laser structure. Selective oxidation of high Al composition Al\textsubscript{x}Ga\textsubscript{1-x}As layers yields a structure with a four period upper Al\textsubscript{x}O\textsubscript{y}/GaAs DBR, a 5.5 period lower Al\textsubscript{x}O\textsubscript{y}/GaAs DBR, and a buried oxide current aperture. A reverse-biased tunnel contact junction provides hole injection via lateral electron current between the upper DBR and the oxide aperture layer. These VCSELs operate with submilliamperes thresholds, high spontaneous efficiencies, and excellent polarization control. © 1998 American Institute of Physics. [S0003-6951(98)03820-0]

The vertical cavity surface emitting laser (VCSEL)\textsuperscript{1} offers various advantages over other light sources, including a symmetrical output beam and ease of manufacturing in the form of two-dimensional arrays. In fact it is now replacing the standard edge-emitting laser and light emitting diode (LED) in many optical data communications applications. Recent advances in VCSELs such as ultralow thresholds\textsuperscript{2} and high efficiencies\textsuperscript{3} have given rise to small linewidths\textsuperscript{4} for VCSELs with compact cavity sizes. Vertical feedback between two mirrors yields a four period upper Al\textsubscript{x}O\textsubscript{y}/GaAs DBR, a 5.5 period lower Al\textsubscript{x}O\textsubscript{y}/GaAs DBR, and a buried oxide current aperture. A reverse-biased tunnel contact junction provides hole injection via lateral electron current between the upper DBR and the oxide aperture layer. These VCSELs operate with submilliamperes thresholds, high spontaneous efficiencies, and excellent polarization control.

The crystal used in this work is grown by low-pressure metalorganic chemical-vapor deposition (MOCVD)\textsuperscript{14} on (100) n-type GaAs substrates misoriented ~2° to the (101) with Se used as the n-type dopant and C as the p-type dopant. Crystal growth begins with a 5.5 period stack of n-type Al\textsubscript{0.95}Ga\textsubscript{0.05}As/GaAs, with buffer layers, that are each ~700 Å of Al\textsubscript{0.70}Ga\textsubscript{0.30}As are grown for bottom-side lateral conduction. The unintentionally doped cavity consists of two ~400 Å Al\textsubscript{0.50}Ga\textsubscript{0.50}As layers sandwiching ~2050 Å of GaAs with two InAs quantum wells (QWs) in the center. A gain peak at λ ~980 nm is intended, but an extra gain peak is also present at ~950 nm. Beyond the cavity a p-type ~500 Å Al\textsubscript{0.95}Ga\textsubscript{0.05}As confining layer, with buffer layers, is grown, and is later oxidized to form the current aperture. Next an ~λ/4 thickness p\textsuperscript{+}/n\textsuperscript{+} GaAs tunnel junction is grown that supplies holes to the active region by lateral electron conduction. The p\textsuperscript{+} (p \geq 10\textsuperscript{20} cm\textsuperscript{-3}) layer is kept thin (~75 Å) to minimize free carrier loss. Finally the structure is completed with a four-period stack of Al\textsubscript{0.95}Ga\textsubscript{0.05}As/GaAs, with buffer layers, which are also ~λ/4 thickness after oxidation.

The VCSELs are fabricated by first defining an ~15 \( \mu \)m diameter disk with photore sist. Then selective wet etching is used to etch through the entire upper DBR, stopping on the tunnel junction. This forms a mesa (a tapered disk) out of the upper DBR that is undercut below the mask to a diameter of ~10 \( \mu \)m at the top and ~15 \( \mu \)m at the bottom. Next, using photolithography and wet etching (H\textsubscript{2}SO\textsubscript{4}:H\textsubscript{2}O\textsubscript{2}:H\textsubscript{2}O 1:8:40), we form an ~48 \( \mu \)m wide trench (~20 \( \mu \)m away from the etched disk), thus exposing the lower DBR for oxidation. An ~24 \( \mu \)m diameter protective disk of photoresist is then centered on the original ~15 \( \mu \)m etched disk, and the...
The SEM image shows a polished section of the tunnel contact VCSEL, leaving an annulus contact region. This prevents shorting in subsequent metallizations. The sample is wet etched again so that the Al$_{0.95}$Ga$_{0.05}$As aperture layer is exposed. This creates an annulus mesa around the upper DBR that allows metal contacting to the tunnel junction. Finally, the sample is placed in a wet oxidation open tube furnace (H$_2$O in a N$_2$ carrier gas) for 55 min at 430 °C to oxidize the high Al composition layers.

Figure 1 shows (a) a top-view optical microscope image of a cleaved sample of the native-oxide-based DBR tunnel contact VCSEL and (b) the corresponding scanning electron microscope (SEM) image (cross section). Although the device is completed [note the “Au” contact pad in (a)], the cross section [Figs. 1(a) and 1(b)] is also convenient in illustrating the fabrication process just through oxidation. The lateral oxidation of the lower DBR [Fig. 1(a)] proceeds from the trench (stubby arrow labeled “Ox”) for a distance of ~40 μm up to the unmarked downward vertical arrow. The lower DBR oxidizes beyond the upper DBR and the contact annulus. In fact it overshoots too far, which only adds resistance. The pair of arrows in Fig. 1(a) marks the diameter of the top layers of the upper DBR (~10 μm) after etching. The SEM image (b) shows that the aperture layer (arrow marked “Ap”) oxidizes underneath the upper DBR from the ~24 μm diameter disk edge, resulting in an aperture diameter of ~7 μm. The upper DBR is completely oxidized, completing the ~2.8 μm thick structure.

After the oxidation process, ~1500 Å of SiO$_2$ is deposited on the crystal everywhere except on the upper DBR and the annulus contact region. This prevents shorting in subsequent metallizations. Ti/Au is evaporated to make metal contact to the tunnel junction, leaving an ~15 μm opening centered on the upper DBR. The crystal is then lapped and polished to ~125 μm thickness, and Ge/Au is evaporated and alloyed to the substrate side of the sample. All measurements are taken at room temperature (300 K) under continuous wave (cw) conditions on diodes mounted epitaxial layer side upward on In-coated copper heat sinks. Power measurements (L–I) are performed in an integrating sphere.

The light versus current (L–I) and spectra (inset) of a native-oxide-based DBR tunnel contact VCSEL are shown in Fig. 2. Some of the VCSELs tested have spontaneous efficiencies as high as 14%. This agrees with data on earlier devices having thin highly defined cavities, and is a result of the more efficient use of the spontaneous emission. The threshold current ($I_{th}$) of the VCSEL of Fig. 2 is ~350 μA, and all the devices tested have thresholds between 250 and 500 μA. Beyond threshold the differential quantum efficiency of the VCSEL is η~20%, which is low but comparable to other VCSELs with similar mirror sets. Decreasing the losses (mirror, free carrier) should increase the efficiency. At 0.1 mA spectral ringing occurs at the cavity resonance, but also an extra gain peak is evident at 950 nm. This is wasted recombination that increases the threshold. At 0.5 mA one mode is present (λ~990 nm), and single mode operation persists until 3×$I_{th}$. The current versus voltage characteristic (data not shown) turns on at 1.2 V, and threshold occurs at 2.2 V. The series resistance is $R_s$ ~800 Ω at $I_{th}$ and 360 Ω at 10×$I_{th}$. The series resistance may be reduced by improved contacting of the top side of the crystal and by reducing the oxidation length of the lower DBR (the “overshoot”).

Figure 3 shows near-field (NF) and far-field (FF) data for the VCSEL of Fig. 2. The NF data on the left show the width of the beam measured parallel to the oxidation trench.
of the device. Below threshold the NF full width at half-maximum (FWHM) is as wide as the Ti/Au metal contact opening. Narrowing occurs at threshold, and the output is single lobed with a minimum width of \(\sim 2.2 \, \mu m\) at 0.7 mA. Widening of the NF occurs with increased excitation. The inset shows the NF image of this device at 1.0 mA, with the trench (not visible) extending vertically in this view. A single spot is shown that is slightly oval, wider in the vertical direction (parallel to the trench). The inset on the far right shows the FF of the device, also measured parallel to the trench direction. The FF pattern is single lobed at 1.0 mA (13\(^\circ\)) and remains fixed up to 3\(I_\text{th}\). Beyond this current side lobes appear, shown here at 1.5 mA (17.5\(^\circ\)). Measuring perpendicular to the trench gives similar but wider FF patterns (14\(^\circ\) at 1.0 mA and 18\(^\circ\) at 1.5 mA), confirming the slightly asymmetric output of the device.

The output polarization of the VCSEL of Figs. 2 and 3 is shown in Fig. 4. The inset shows (nonmetallized VCSEL) \(E_\parallel\) and \(E_\perp\) defined with respect to the oxidation trench. The \(L-I\) curves show that the laser output is polarized in the \(E_\parallel\) direction, with the \(E_\perp\) direction producing only spontaneous light. All of the VCSELs exhibit this behavior. The polarized output persists up to the maximum output power of the device. Polarization control has been achieved with oval-apertured VCSELs previously,\(^3\) but with the polarization aligned with the longer axis of the aperture. Here the opposite occurs, which suggests that another feature determines the polarization. The oxidation of the lower DBR from a trench produces a natural asymmetry in the device. The oxidation process proceeds from the trench tapering (shrinking) slightly, thus creating a slight detuning of the lower DBR and cavity horizontally away from the trench. Also, the oxidation undoubtedly induces stress. Additionally, current on the bottom side of the VCSEL flows in the same direction that the light is polarized, perpendicular to the trench, and may influence the polarization. One or all of these contribute to the polarization control.

Finally, compact VCSELs (total thickness \(\sim 2.8 \, \mu m\)) have been achieved with the use of native-oxide-based DBRs, buried oxide apertures, and thin \(n\)-type GaAs lateral current-feed layers augmented with a tunnel contact junction on the \(p\) side to supply hole injection. These devices display the high spontaneous efficiencies characteristic of other thin cavity devices, and exhibit low current thresholds despite the nonideal gain profile. Also, the form of the device leads to complete polarization control. Since the lateral conducting layers used in these VCSELs are thin, more compact structures can be achieved in further work by resorting to "one-\(\lambda\)" cavities to make even more efficient use of the spontaneous emission (\(I < I_\text{th}\)).

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